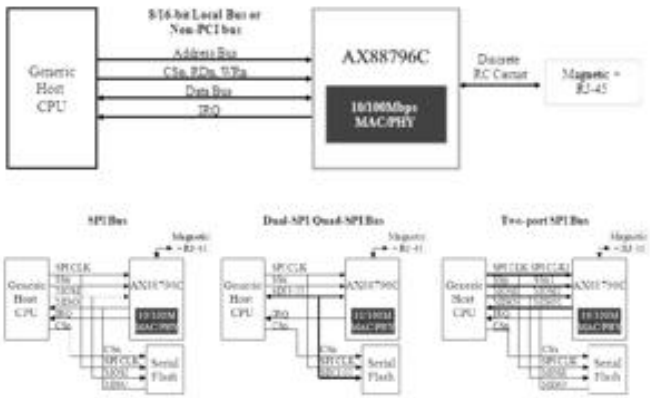
Spoločnosť ASIX Electronics Corporation predstavila novú variantu v ponuke embedded ethernet produktov.Jedná sa o AX88796C - low-power Fast Ethernet MAC + PHY.Pripojiteľnosť k MCU je pomocou SPI zbernice, alebo adresno/dátovej (nie PCI) zbernice. Cenu a dostupnosť som nezistil. Firma Codico, oficiálny distribútor ASIX EC, evidentne nechce a **nereaguje na emaily**.
Ale priamo z firmy ASIX mi odpísali....
Tento čip umožní jednoducho pridať mikrokontrolérom ethernet konektivitu. Asix čip nie je veľký (LQFP 64), je IEEE 802.3/802.3u 10BASE-T/100BASE-TX kompatibilný a podporuje režim zníženej spotreby s možnosťou WOL (wake-on-lan) prebudenia.

Vlastnosti

- High-performance non-PCI local bus
  - Supports 8/16-bit SRAM-like host interface (US Patent Approval), easily interfaced to most common embedded MCUs; or 8/16-bit local CPU interface including MCS-51 series, Renesas series CPUs
  - Supports Slave-DMA to minimize CPU overhead and burst mode read & write access for frame reception & transmission on SRAM-like interface for high performance applications
  - Supports multi-frames burst transfer mechanism to increase bulk DMA transfer size and reduce CPU loading due to frequent interrupts for short frame reception/transmission (US Patent Pending). The patented “short frame early dispatch timer” provides programmable delay for short packet transfer latency control. Supports padding bytes insertion between frames within a multi-frame burst for double word boundary alignment
  - Supports variable voltage I/O (1.8/2.5/3.3V) and programmable driving strength (8/16mA)
  - Interrupt pin with programmable timer
- High-performance SPI slave interface
  - Supports SPI slave interface for CPU with SPI master. The SPI slave interface supports SPI timing mode 0 and 3, up to 40MHz of SPICLK, variable voltage I/O and programmable driving strength
  - Supports Quad-SPI or Dual-SPI flash memory interface for high performance applications Supports RX Buffer Ring and TX Buffer Ring structure to receive or transmit or simultaneously receive and transmit packets from/to the MAC RX/TX packet buffer in burst transfer mode. Also supports multi-frames burst transfer mechanism to increase bulk DMA transfer size and reduce CPU loading due to frequent interrupts for short frame receive/transmission (US Patent Pending)
  - Supports Two-Port SPI interface to increase bandwidth
  - Supports optional Ready signal as flow control for SPI packet RX/TX
- Single-chip Fast Ethernet MAC/PHY controller
  - Embeds 14KB SRAM for packet buffers
  - Supports IPv4/IPv6 packet Checksum Offload Engine to reduce CPU loading, including IPv4 IP/TCP/UDP/ICMP/IGMP and IPv6 TCP/UDP/ICMPv6 checksum generation & check
  - Supports VLAN match filter
  - Integrates IEEE 802.3/802.3u standards compatible 10BASE-T/100BASE-TX (twisted pair copper mode) Fast Ethernet MAC/PHY transceiver in one single-chip
  - Supports twisted pair crossover detection and correction (HP Auto-MDIX)
  - Supports full duplex operation with IEEE 802.3x flow control and half duplex operation with back-pressure flow control
  - Supports auto-polling function
  - Supports 10/100Mbps N-way Auto-negotiation operation

- Advanced Power Management features
  - Supports dynamic power management to reduce power dissipation during idle or light traffic period
  - Supports very low power Wake-On-LAN (WOL) mode when the system enters sleep mode and waits for network event to awake it up. The wakeup events supported are network link state change, receipt of a Magic Packet or a pre-programmed Microsoft Wakeup Frame or through GPIO pin
  - Supports Protocol Offload (ARP & NS) for Windows 7 Networking Power Management
  - Supports complete I/O pins isolation during WOL mode or Remote Wakeup Ready mode to reduce leakage current on non-PCI and SPI slave host interface
  - Supports three Power Saving Modes with Energy Detect during Ethernet cable unplug configured either by software or hardware automatically
- Supports optional EEPROM interface to store MAC address
- Supports up to four GPIOs and two of them support Wake-On-LAN Supports programmable LED pins for various network activity indications with variable voltage I/O and programmable driving strength
- Integrates voltage regulator, 25MHz crystal oscillator and power on reset circuit on chip
- Supports optional clock output (25, 50, or 100MHz) for system use, if 25MHz crystal is present
- Supports alternative clock input (25MHz) from system clock to save the 25MHz crystal cost
- 64-pin LQFP RoHS compliant package
- Operates over 0 to +70□C or -40 to +85□C temperature range

Aplikačné zapojenie



Cena, dostupnosť

Upravené 25.03.2010

Už nečakám na vyjadrenie distribútora....

Z firmy ASIX som dostal odpoveď, v ktorej sa uvádza, že pokiaľ chcem cenu zverejniť, tak mi ju nemôžu prezradiť (majú málo vyrobených na sklade, boja sa hromadného nákupu...). Ale inak že ich teší môj záujem o produkty, a mám sa kľudne pýtať aj ďalej.

Hmm, aspoň NEJAKÁ odpoveď.
btw. CODICO neodpovedá ani z centrály.

Odkazy
AX88796C homepage

Distribúcia
viď. Adresár

12/03/2010 14:54:51
1 úprava: 22/03/2010 14:14:46