Interfacing Virtex-6 FPGAs with 3.3V I/O Standards
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Introduction

All the devices in the Virtex®-6 family are compatible with and support 3.3V I/O standards. This application note describes methodologies for interfacing Virtex-6 devices to 3.3V systems. It covers input, output, and bidirectional busses, as-well-as signal integrity issues and design guidelines.

The Virtex-6 FPGA I/O is designed for both high performance and flexibility. Each I/O is homogenous, meaning every I/O has all features and all functions. This High-performance I/O allows the broadest flexibility to address a wider range of applications. A range of options can be deployed to interface Virtex-6 FPGA I/O to 3.3V devices.

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