Maxim uviedol novinku, ktorá možno zrevolucionalizuje modernú a prudko sa rozvíjajúcu oblasť umelej inteligencie.

MAX78000 je mikrokontrolér, ktorý má zaintegrovanú zaujímavú jednotku pre implementáciu neurónových sietí. Jedná sa vlastne o 64 špecializovaných procesorov s prístupom k 512kB RAM. Keďže o neurónových sietiach a umelej inteligencii vie priemerný čitateľ mikroZone pravdepodobne viac než redaktori, obmedzíme sa tu na vymenovanie vlastností tejto jednotky:

Vlastnosti

- 512KB SRAM data storage
  - Configured as 8Kx8-bit integers x64 channels or 32Kx8-bit integers x4 channels for input layers
  - Hardware load and unload assist
- 64 parallel physical channel processors
  - Organized as 4x16 processors
  - 8-bit integer data path with option for 32-bit integers on the output layer
  - Per-channel processor enable/disable
  - Expandable to 1024 parallel logical channel processors
- 1x1 or 3x3 2D kernel sizes
- Configurable 1D kernel size to 1x9
- Full resolution sum-of-product arithmetic for 1024 8-bit integer channels
- Operating frequency up to 50MHz
- Nominal 1 output channel per clock, maximum 4 output channels per clock (passthru)
- Configurable input layer image size
  - 32K pixels, 16 channels, non-streaming
  - 8K pixels, 4 channels, non-streaming
  - 1024 x 1024 pixels, 4 channels, streaming
- Hidden layers
  - Up to 8K 8-bit integer data per channel, x64 channels, non-streaming
  - 8K bytes can be split equally across 1 to 16 logical channels, non-streaming
  - 1M 8-bit integer data per channel, x64 channels, streaming
  - 1M bytes can be split equally across eight layers, streaming
- Optional interrupt on CNN completion
- User-accessible BIST on all SRAM storage
- User-accessible zeroization of all SRAM storage
- Single-step operation with full data SRAM access for CNN operation debug
- Flexible power management
  - Independent x16 processor supply enables
  - Independent x16 processor mask retention enables

- Independent x16 data path clock enables
- Active Arm peripheral bus clock gating with per x16 processor override
- CNN clock frequency scaling (divide by 2, 4, 8, 16)
- Chip-level voltage control for performance power optimization

- Configurable weight storage
  - SRAM-based weight storage with selectable data retention
  - Configurable from 442K 8-bit integer weights to 3.456M 1-bit logical weights
  - Organized as 768X9X64 8-bit integer weights to 768x72x64 1-bit logical weights
  - Can be configured on a per-layer basis
  - Programmable per x16 processor weight RAM start address, start pointer, and mask count
  - Optional weight load hardware assist for packed weight storage

- 32 independently configurable layer groups
  - Each group can contain element-wise, and/or pooling, and/or convolution operations for a minimum of 32 and a maximum of 96 layers
  - Processor and mask enables (16 channels)
  - Input data format
  - Per-layer data streaming
  - Stream start - relative to prior stream
  - Dual-stream processing delay counters - 1 column, 1 row delta counter
  - Data SRAM circular buffer size
  - Input data size (row, column)
  - Row and column padding 0 to 4 bytes
  - Number of input channels 1 to 1024
  - Kernel bit width size (1, 2, 4, 8)
  - Kernel SRAM start pointer and count
  - Inflight input image pooling
  - Pool mode - none, maximum or average
  - Pool size - 1x1 to 16x16
  - Stride - 1 row, 1 column to 4 rows, 4 columns
  - Data SRAM read pointer base address
  - Data SRAM write pointer configuration
  - Base address

- Independent offsets for output channel storage in SRAM

- Programmable stride increment offset

- Bias - 2048 8-bit integers with option for 512 32-bit integers

- Pre-activation output scaling from 0 to 8 bits

- Output activation - none, ReLU, absolute value

- Passthru - 8-bit or 32-bit integers

- Element-wise operations (add, subtract, xor, or) with optional convolution - up to 16 elements

- Deconvolution (upscaling)

- Flattening for MLP processing

- 1x1 convolution

A ak by niekoho tento zoznam predsalen neohúril, MAX78000 obsahuje ešte jedno prekvapenie. Ste nerozhodnutí, či máte ako hlavný procesor použiť ARM (Cortex-M4) alebo RISC-V? Nevadí! MAX78000 totiž obsahuje oboje!

ARM Cortex-M4+FPU beží do 100MHz, RISC-V do 60MHz.

A okrem toho obligátna sadu periférií:

- 512kB FLASH

- 128kB SRAM (z toho 32kB má ECC, a 16kB sa dá konfigurovať ako inštrukčná cache pre RISC-V); z datasheetu to nie je úplne jasné ale zdá sa, že aj ARM jadro má 16kB inštrukčnú cache

- 3x I2C, 3x UART, 2x SPI, I2S, 1-Wire master, 4x pulse train engines, 4x 32-bit timers, 2x LP timers

- DMA

- 2x watchdog

- parallel camera interface (lebo AI je aj rozoznávanie obrazu)

- 8-channel 10-bit sigma-delta ADC, 4x comparator

- AES, CRC, true RNG

- sada hodín, vrátane RTC

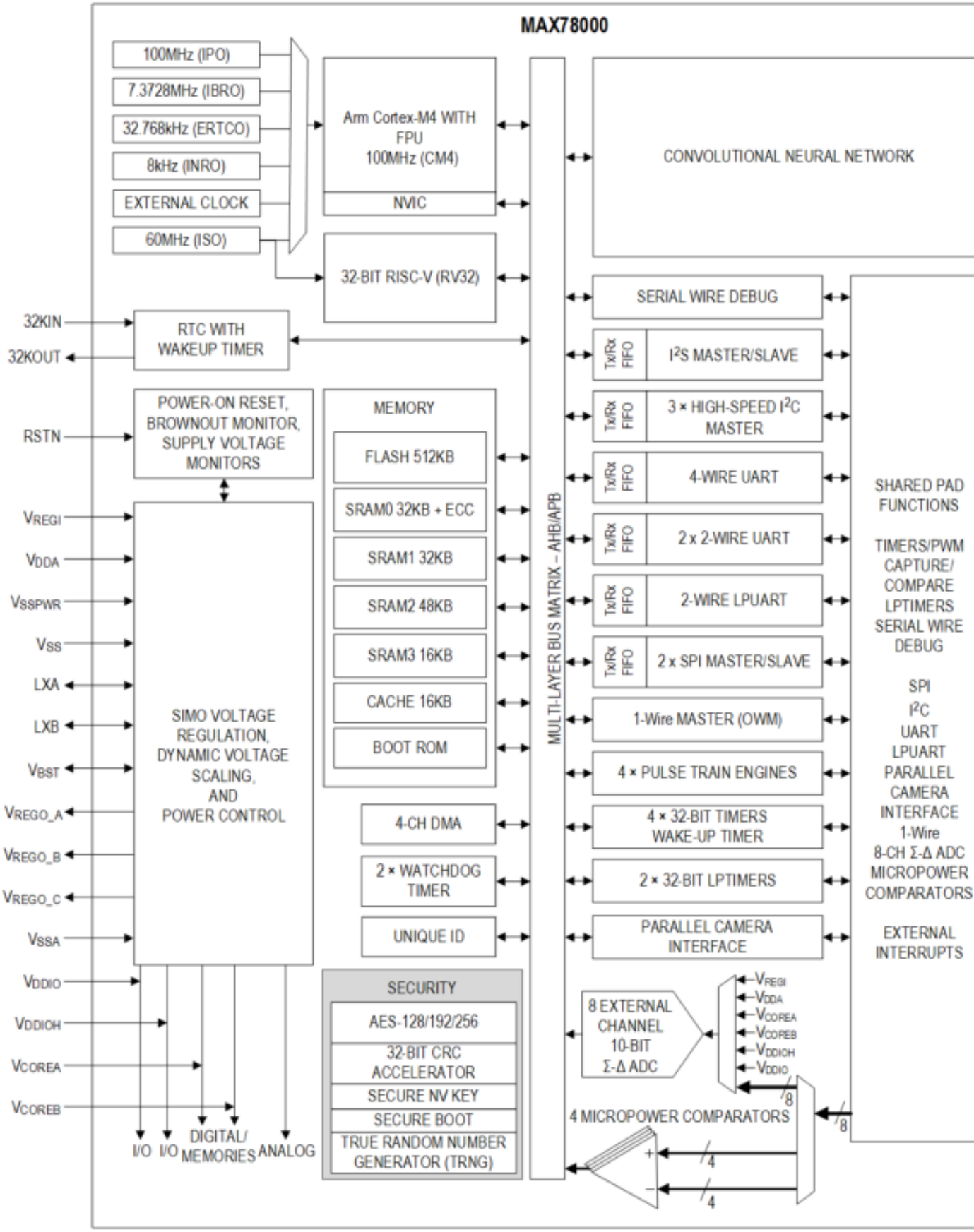
- reset+brownout, SWI debug

- napájacia jednotka vrátane viacvýstupového spínaného zdroja s jednou cievkou (SIMO)

Samozrejmosťou je dnes sada režimov s nízkou spotrebou a zabudovaný bootloader.

MAX78000 sa dodáva len v jedinom nechutnom 81-pinovom BGA puzdre s roztečou 0.8mm.

Blokové zapojenie



Cena

MAX78000 stojí okolo $20 (samozrejme podľa množstva), a aj v aktuálnej mizérii s polovodičmi sa dá v množstve pár desiatok až stoviek kusov kúpiť takmer u všetkých bežných distribútorov.

Okrem toho je k dispozícii aj "lacná jednoduchá" vývojová doska MAX78000 FEATHER BOARD za ľudových $30.

A pre fajnšmekrov je tu aj plnohodnotný EVALUATION BOARD za dve stovky.

Odkazy
Stránka produktu